Abstracts

A novel dimension-reduction technique for the capacitance extraction of 3-D VLSI interconnects

Wei Hong, Wei-Kai Sun, Zhen-Hai Zhu, Hao Ji, Ben Song and W.W.-M. Dai. "A novel dimension-reduction technique for the capacitance extraction of 3-D VLSI interconnects." 1998 Transactions on Microwave Theory and Techniques 46.8 (Aug. 1998 [T-MTT]): 1037-1044.

In this paper, a new capacitance extraction method called the dimension-reduction technique (DRT) is presented for three-dimensional (3-D) very large-scale integration (VLSI) interconnects. The DRT converts a complex 3-D problem into a series of cascading simple two-dimensional (2-D) problems. Each 2-D problem is solved separately, thus we can choose the most efficient method according to the arrangement of conductors. We have used the DRT to extract the capacitance matrix of multilayered and multiconductor crossovers, bends, vias with signal lines, and open-end. The results are in close agreement with those of Ansoft's SPICELINK and the Massachusetts Institute of Technology's (MIT) FastCap, but the computing time and memory size used by the DRT are several (even ten) times less than those used by SPICELINK and FastCap.

❑ Return to main document.